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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,553	08/30/2001	Michael L. Frank	10010472-1	3086
22878	7590	03/03/2004	EXAMINER	
AGILENT TECHNOLOGIES, INC. INTELLECTUAL PROPERTY ADMINISTRATION, LEGAL DEPT. P.O. BOX 7599 M/S DL429 LOVELAND, CO 80537-0599			NGUYEN, KHAI M	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/944,553

Applicant(s)

FRANK, MICHAEL L.

Examiner

Khai M. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 5-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 5-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Allowable Subject Matter***

1. The indicated allowability of claims 5-21 is withdrawn in view of the newly discovered reference(s) to US Publication No. US 2002/0034934 A1 in view of US Patent No. 5,949,299. Rejections based on the newly cited reference(s) follow.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 5-6, 9, 13-15, 17-19, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe et al. (US 2002/0034934 A1).

Regarding claim 5, Watanabe et al. discloses a component (10, see Figs. 1-5) comprising a balun circuit (13, 14) and a filter circuit (11) with a single-ended input and a single-ended output (101, 112) are integrated in a multilayer substrate (15 of Fig. 5).

Regarding claim 6, Watanabe et al.'s filter (11) is resonator-based filter (Fig. 2).

Regarding claim 9, Watanabe et al. discloses a component (10 of Fig. 1) comprising a balun circuit(s) including at least two transmission lines (Figs. 4A and 4B) (13 and/or 14) which is/are integrated with a filter circuit (11) in a multilayer substrate (15; see Figs. 5, 6A-8B; and [0067]-[0068]).

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Regarding claim 12, Watanabe et al. discloses a component comprising a balun (13, 14) that is integrated with a resonator filter/FBAR filter/half ladder filter (11; Fig. 2) in a multilayer substrate (15) to form a single component (10; see Figs. 1-7D).

Regarding claim 13, Watanabe et al. discloses a component (10, see Figs. 1-5) comprising a filter circuit (11) with a single-ended input and a single-ended output (101, 112) and a balun circuit (13, 14), having single-ended ports and differential ports, are integrated in a multilayer substrate (15; see Figs. 5, 6A-7D).

Regarding claims 14, and 18, the component (10) of Watanabe et al. comprises a single-ended input (101), a differential output (104-105), a first stage (11), and second stage (14) coupled to the first stage (11) via a coupling stage (12), wherein the filter (11) is in the first stage; wherein the single-ended input (101) of the filter (11) is coupled to the single-ended input of the component (10); wherein the balun (14) is in the second stage; wherein the single-ended port of the balun (141) is coupled to the single-ended output port of the filter (11); and wherein the differential port of the balun (104-105) is coupled to the differential output of the component (10) (see Fig. 1).

Regarding claim 15, and 19, the component (10) of Watanabe et al. (Fig. 1) comprises a differential input (102-103), a single-ended output (101) a first stage (13), and a second stage (11) coupled to the first stage via a coupling stage (12); wherein the balun (13) is in the first stage; wherein the differential port (102-103) of the balun (13) is coupled to the differential input of the component (10); wherein the filter (11) is in the second stage; wherein the single-ended input (121) of the filter is coupled to the single-

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ended port of the balun (131); and wherein the single-ended output of the filter (101) is coupled to the single-ended output of the component (10).

Regarding claim 17, Watanabe et al. discloses a filter (11) that is integrated with balun circuits (13, 14) in a multilayer substrate (15) to form a single component (10) including single-ended and differential input/output ports, which provides a filter function and a balun function.

Regarding claim 21, Watanabe et al. discloses a component (10, see Figs. 1-5) comprising a balun circuit (13, 14), and a filter circuit (11) that is integrated with the balun(s), and wherein the balun and filter are bonded together in a multilayer substrate (15; see Figs. 5, 6A-7D).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 7-8, 10-11, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 2002/0034934 A1) in view of Harada (US 5,949,299).

Regarding claims 7-8, Watanabe et al. discloses a filter (11) that is integrated with balun circuits (13, 14) in a multilayer substrate (15) to form a single component (10), which provides a filter function and a balun function of the claimed invention except for a different type of filter was used. It would have been obvious to one person

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having ordinary skill in the art at the time the invention was made to substitute the resonator-base filter (11) with a full-ladder resonator-based filter and a lattice resonator-based filter since these filters are known and the selection of any of these known filters would be within the level of ordinary skill in the art.

Regarding claims 10-11, Watanabe et al. discloses the component of claimed invention, *including a balun circuit (13, 14) that is integrated with a filter (11) in a multilayer substrate (15) to form a single component (10); input ports; output ports; and two elements (13, 14) for performing impedance transformation at the input/output ports*, except for the balun is implemented with lumped elements that includes inductors and capacitors. Harada discloses a balun circuit (1A-2H) comprising lumped elements is known for reducing the side and mass of a multilayer structure component. Therefore, it would have been obvious to one person having ordinary skill in the art at the time the invention was made to implement the balun circuit as taught by Watanabe et al. with inductors and capacitors to reduce the chip area of the component (see column 2, lines 9-15).

Regarding claims 16 and 20, Watanabe et al. discloses the component of claimed invention of claim 13, including a half-ladder/FBAR filter, except for a different type of balun was used. Harada discloses a balun circuit (1A-2H) comprising lumped elements is known for reducing the side and mass of a multilayer structure component and the FBAR filter and/or SAW filter are also known. Therefore, it would have been obvious to one person having ordinary skill in the art at the time the invention was made to implement the balun circuit as taught by Watanabe et al. with inductors and capacitors to reduce the chip area of the component (see column 2, lines 9-15).

***Prior Art***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (see attached PTO 892).


***Contact Information***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 8:00 to 4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN

  
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